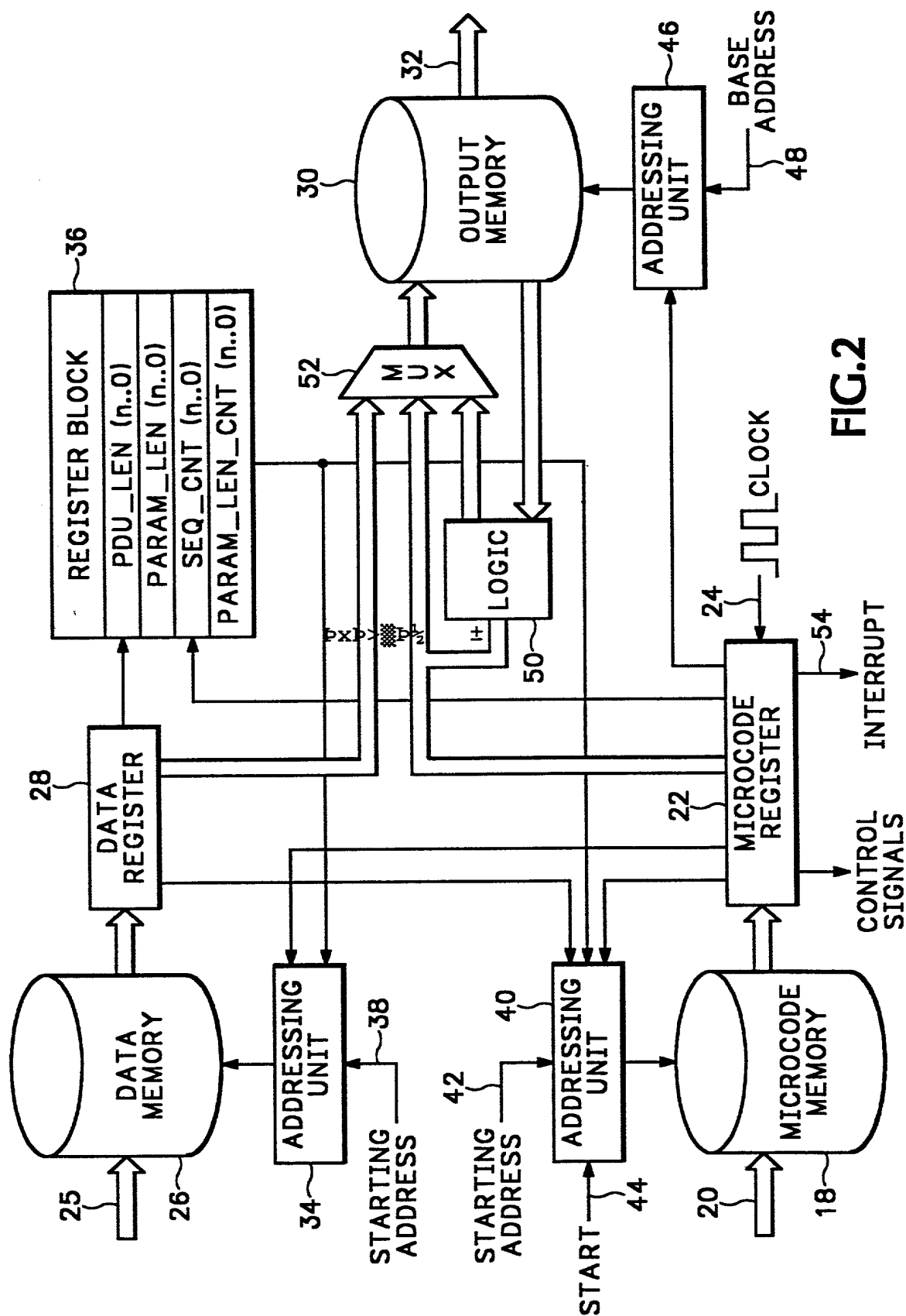


```
graph TD; 14[COMMAND DECODER] --> 16[ADDRESSING LOGIC]; 14 --> 12[CONTROL REGISTER]; 16 --> 10[(MICROPROGRAM MEMORY)]; 10 --> 12; 12 --> CS[CONTROL SIGNALS];
```

FIG. 1

FIG.1



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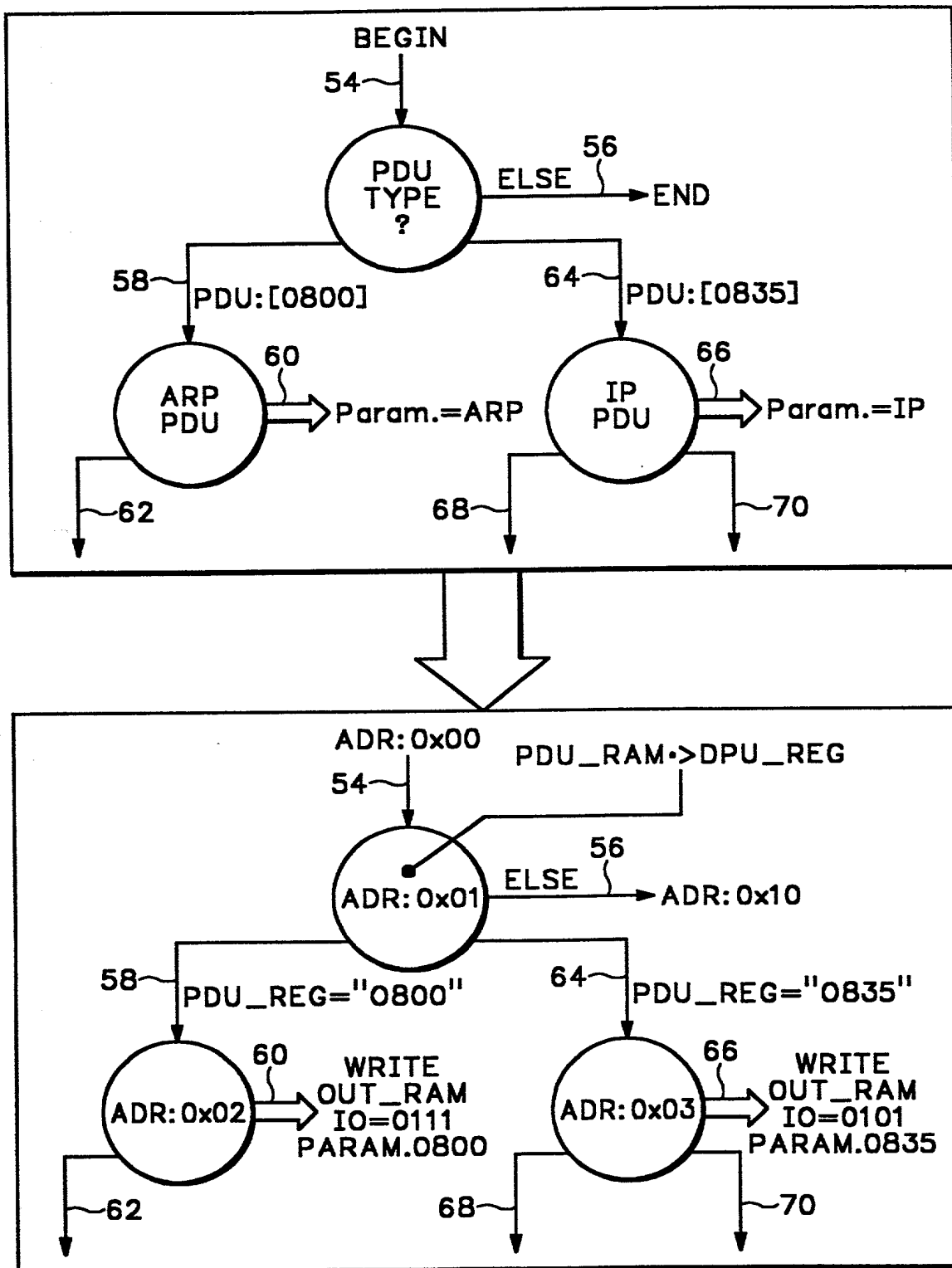


FIG.3